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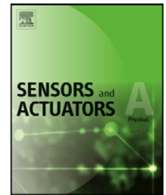

# Hemispherical thin-film transistor passive pixel sensors

Geonwook Yoo [a], Tze-ching Fung [a], Daniela Radtke [b], Marko Stumpf [b], Uwe Zeitner [b], Jerzy Kanicki [a,*]

[a] EECS Department, University of Michigan, Ann Arbor, MI 48109, USA
[b] Fraunhofer Institute for Applied Optics and Precision Engineering, Jena, Germany

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ABSTRACT

Hemispherical image sensors are very promising technology for cameras, surveillance systems and artificial vision. We report on the electrical performance of the hydrogenated amorphous silicon thin-film transistor passive pixel image sensor (PPS) circuits fabricated on a hemispherical substrate using maskless laser-write lithography (LWL). The level-to-level registration and alignment over the curved surface with a high accuracy are demonstrated for the LWL in this work. The obtained results clearly show that it is possible to realize active-matrix PPS with a 150 μm pixel pitch and a dynamic range of about 40 dB that is suitable for hemispherical image sensors.

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## 1. Introduction

Complementary metal oxide semiconductor (CMOS) image sensors based on the active pixel sensor concept are used in mobile-imaging, digital and video cameras. They have a high speed, wide dynamic range and low power-consumption [1]. For large area applications such as security scanning and medical imaging, the hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) flat panel imagers based on passive pixel sensor (PPS) concept are used [2–4]. So far, all current state-of-the-art image sensor technology has been developed on flat surfaces. Recently, due to the unique advantages of the hemispherical image sensor such as a wide field of view (FOV) and low aberrations with less optical and mechanical components in the system [5], various strategies have been proposed to implement optoelectronic devices on non-planar surfaces. They are crucial to realize imaging systems on a hemispherical surface [6–13]. Although all the proposed methods have demonstrated feasibility and a working hemispherical sensor [6], they are not adequate to realize active-matrix high resolution pixel arrays. These strategies are limited by the lack of scaling capability [6,9–11], strain by deformation [7,8] and a poor level-to-level alignment accuracy [12,13]. As an alternative to circumvent these limitations, a direct fabrication method using optical lithography has been considered [6]. In the past the maskless laser-write lithography (LWL) system was used to fabricate the micro-optical elements on both concave and convex glass lenses at a single-mask level [14,15]. In this paper, we demonstrate the feasibility of using LWL with level-to-level alignment capability needed to realize a high performance a-Si:H TFT PPS. We then describe the electrical performance of the fabricated PPS circuits on a hemispherical glass substrate.

## 2. Experimental details and testing set-up

Fig. 1 shows a picture of the fabricated PPS circuits consisted of the bottom-gate structure a-Si:H TFT switch (SCAN) and a storage capacitor ($C_{ST}$) on a concave substrate. The elongated connection lines among the TFT, capacitor and contact pads were intended for checking the uniformity of TFT circuit fabricated over the curved surface. Prior to the LWL exposure step for each level, the photoresist (AZ1505) was spin-coated to form a uniform coating over the curved surface; the ratio of substrate-radius (0.865 cm) to radius-of-curvature (3 cm) is below 0.816, which guarantees for the spin-coated film to be in nearly homogeneous composition over the curved surface [16,17]. The level-to-level alignment error is defined as the relative position deviation of the alignment marks within the two layers placed on top of each other. We derived vertical and horizontal deviation from the measurement of the distance of the borders on four sides in the bar alignment mark. The measured error was less than 2 μm for the TFT with 10 μm channel length and up to the 300 μm channel width. More details about the a-Si:H TFT processing using the LWL on a hemispherical surface can be found elsewhere [17].

Fig. 2(a) shows a schematic of the circuit that is electrically tested using home-made external readout electronics consisted of a Burr-Brown 102 charge amplifier with a feedback capacitor ($C_{FB}$) of 10 pF. The schematics of the driving waveforms and simu-

* Corresponding author. Tel.: +1 734 936 0964; fax: +1 734 615 2843.
*E-mail address:* kanicki@eecs.umich.edu (J. Kanicki).

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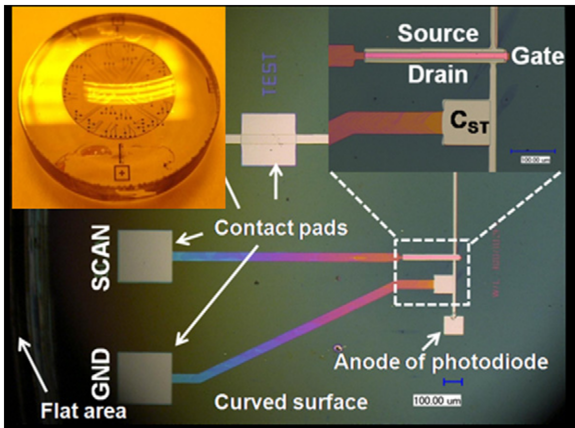


**Fig. 1.** Photograph of the fabricated substrate and optical micrograph of the pixel sensor circuit at the edge of the curved surface. (Inset) Detailed micrograph of the a-Si:H TFT and $C_{ST}$.

lated results of output voltage, $V_{OUT}$ $(t)$ using HSPICE are given in Fig. 2(b). To accurately compare and predict performances of the fabricated PPS on the curved surface, we fitted the measured data into LEVEL 61 RPI a-Si TFT model [18] and then extracted all needed TFT parameters for the simulation. Electrical measurements of the TFT were conducted and analyzed using a HP 4156 semiconductor parameter analyzer. To evaluate the electrical performance of the PPS, we used a Keithley 6221 DC/AC current source to generate test current ($I_{TEST}$). This current is used to mimic the light-modulated current, which will be generated from the photodiode (see gray box of Fig. 2(a)). We would like to discuss briefly about the feasibility of photodiode fabrication on the curved surface. An inorganic photodetector layer, e.g. a-Si photodiode [3], can be formed on top of the PPS circuit by PECVD and then be patterned using the same LWL

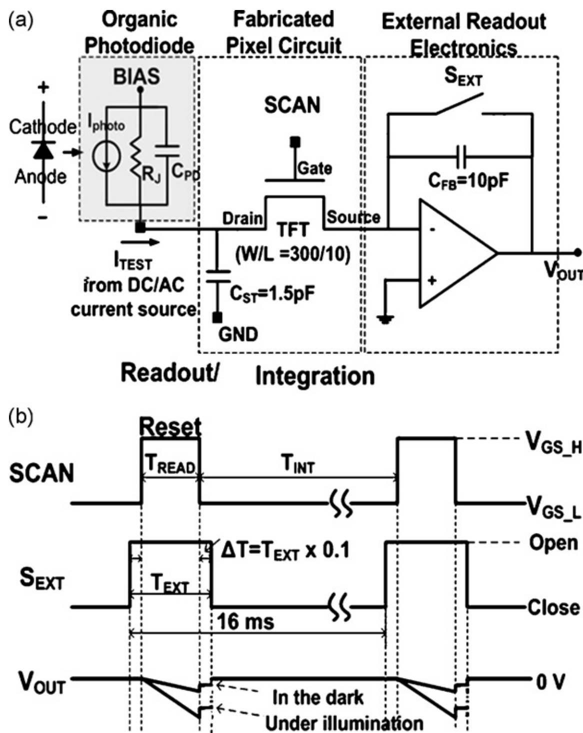


**Fig. 2.** (a) Schematic of the pixel sensor circuit with external readout electronics used in the electrical testing. The gray box indicates the organic photodiode which is not integrated in this experiment. (b) Schematic of the driving waveforms and simulated result of $V_{OUT}$.

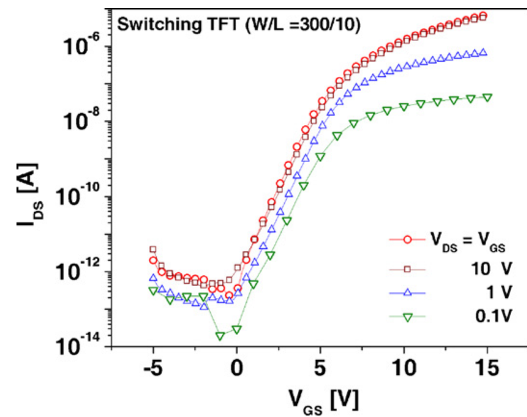


**Fig. 3.** Transfer characteristics of the switching TFT for various $V_{DS}$.

method. An alternative approach, as demonstrated by Tedde et al. [19], is using a solution-processable organic photodetector (OPD) that will allow us to fabricate a photosensor on the curved surface using spin-coat. OPD integration enables us to achieve a high fill factor close to 100%. However, for a high resolution array processing, this continuous sensor design may bring about undesirable issues such as parasitic capacitance and lateral cross-talk between pixels [20].

The light-modulated current from the photodiode is given by the equation:

$$I_{TEST} = I_{photo} = \frac{P_{in} \times \eta_{ext} \times e}{h\upsilon} \quad (1)$$

where $e$ is unit charge, $\eta_{ext}$ is external quantum efficiency and $h\upsilon$ is the light photon energy. Assuming the organic photodetector is integrated on top of the PPS [19], for a range of the light intensity from 0 to 0.36 mW/cm$^2$ we estimated corresponding $I_{TEST}$ (=$I_{photo}$) range from 0 to 2.1 nA. Considering the frame rate of 60 Hz and 100 × 100 pixel arrays, we set the integration time ($T_{INT}$) and the read time ($T_{READ}$) to ∼16 ms and 128 μs, respectively. The switch in the external readout circuits ($S_{EXT}$) is open for a period of external integration time ($T_{EXT}$) of 160 μs; we added a 10% offset (16 μs) into the $T_{EXT}$ to fully open the $S_{EXT}$ before SCAN is closed so that no signal is lost. A 10% offset (16 μs) is also included into the $T_{EXT}$ after SCAN is open to measure stable $V_{OUT}$.

### 3. Measurements and discussions

Based on 10–90% data range of the maximum drain-to-source current, the extracted parameters of the TFT switch ($W/L$ = 300/10) in a linear operation regime were as follows: field-effect mobility ($\mu_{FE}$) ∼0.11 cm$^2$/V s, threshold voltage ($V_{th}$) ∼5.06 V, OFF current ($I_{OFF}$) at $V_{GS}$ = −5 V ∼0.32 pA, and subthreshold swing (SS) ∼1.07 V/dec (see Fig. 3). The ON/OFF current ratio was ∼10$^6$ and the ON-state resistance of TFT switch ($R_{ON}$) derived from linear operation characteristics was 4.1 MΩ at $V_{GS}$ = 10 V. $C_{GD}$ and $C_{GS}$ were calculated to be 112 fF ($W/L$ = 300/10) for an overlap of 4 μm between the gate and drain electrodes, and between the gate and source electrodes, respectively.

The charge transfer time ($\tau$) through SCAN is given by $\tau = C_{PIXEL} \times R_{ON}$, where $C_{PIXEL}$ is the sum of $C_{GD}$, $C_{ST}$ and photodiode capacitance ($C_{PD}$). By integrating the organic photodetector [19] on top of 150 μm pixel pitch PPS, we estimated the $C_{PD}$ to be about 3.8 pF for corresponding $C_{PIXEL}$ = 5.4 pF. Finally, $\tau$ is calculated to be ∼22 μs. For 99.3% charge readout on $C_{PIXEL}$, five time constants of $\tau$ (∼110 μs) is sufficient [21]. The calculation result shows that 100 × 100 pixel arrays with 60 Hz frame based on column-parallel readout can be realized. To realize higher resolution arrays (e.g.

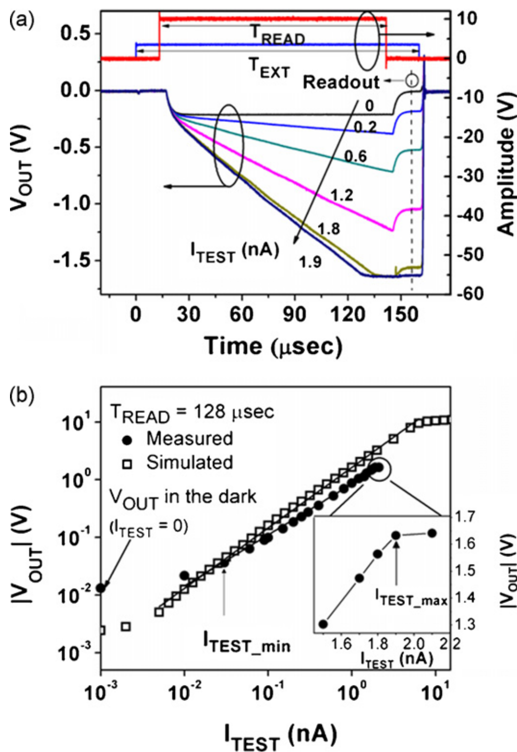


**Fig. 4.** (a) Oscilloscope traces of $V_{OUT}$ for different $I_{TEST}$. (b) Solid circles show the linearity plot of the measured $V_{OUT}$ vs. $I_{TEST}$ by sampling $V_{OUT}$ at 158 μs. (Inset) Non-linearity is shown at high values of $I_{TEST}$. Squares show the simulated results.

1000 × 1000) with the same pixel pitch and frame rate, we need smaller $R_{ON}$ to achieve shorter $\tau$. So the a-Si:H active layer needs to be replaced with a thin-film channel material having a higher field-effect mobility such as amorphous indium gallium zinc oxide (a-IGZO) [22].

During the PPS operation, TFT thermal and flicker noise can both affect the pixel performance. The TFT thermal noise commonly characterizes as "white noise" with a constant noise spectral density. On the other hand, spectral density for flicker noise has $1/f$ dependence and is only significant in low frequency range. For a-Si:H TFT, the corner frequency for its flicker noise has been measured to be around 100 Hz [23]. Because of the short readout time ($T_{READ}$ = 128 μs), there is a low frequency cut-off (cut-off frequency ∼8 kHz) in our PPS circuit and such low frequency cut-off filters out most of the TFT flicker noise. Therefore, the dominant component of PPS noise among various noise sources (i.e. flicker, thermal, etc.) is $kTC$ noise, and it can be estimated using the formula: $\sigma_{PPS} = (kTC_{PIXEL})^{1/2}$ [24]. In the above equation, $k$ is the Boltzmann constant and $T$ is the Kelvin temperature. With $C_{PIXEL}$ of 5.4 pF, the PPS noise represented as charge fluctuation ($\sigma_{PPS}$) at room temperature (300 K) is ∼940 electrons. With the readout/reset time ($T_{READ}$) of 128 μs, the equivalent noise current is calculated to be ∼1.2 pA. Hence it is important that TFT $I_{OFF}$ is less than 1 pA.

Oscilloscope traces of $V_{OUT}$ for various $I_{TEST}$ are shown in Fig. 4(a). $I_{TEST}$ = 0 nA corresponds to no light-modulated current, and $V_{OUT}$ starts to saturate at $I_{TEST}$ = 1.9 nA due to the complete discharge of $C_{ST}$ (1.5 pF) during the readout. Furthermore, to characterize the dynamic range (DR) which quantifies sensor's ability to image scenes with the wide spatial variations in illumination [25], we evaluated the linearity of $V_{OUT}$ in response to $I_{TEST}$ for the range of 0.01–2.1 nA by sampling the stabilized $V_{OUT}$ at 158 μs (Fig. 4(b)). The dynamic range is given by the equation:

$$\text{Dynamic range (DR)} = 20 \times \log\left(\frac{I_{max}}{I_{min}}\right), \quad (2)$$

where $I_{max}$ is a maximum non-saturated signal and $I_{min}$ is a minimum detectable signal. Fig. 4(b) shows the saturation effect for the $I_{TEST}$ corresponding to high light intensities. DR was measured to be about 40 dB for the fabricated PPS.

Simulated result of DR is also shown in Fig. 4(b). Simulated $V_{OUT}$ is slightly higher than measured values because an ideal Op-amp is used in the simulation and there is no current loss by flowing into the input of the Op-amp. For simulated data DR is calculated to be about 60 dB. The low end of $V_{OUT}$ is affected by the leakage current of SCAN ($I_{OFF}$, 0.32 pA) and reset noise (∼1.2 pA) [25]. Since the simulation result using HSPICE does not include noises from SCAN and DC/AC current source, lower $I_{TEST}$ (∼5 pA) can be detected. The high end of $V_{OUT}$ is limited by $C_{PIXEL}$ for given $T_{INT}$ [25]. Designed capacitances of $C_{ST}$ and $C_{GD}$ constituting $C_{PIXEL}$ are subject to insulator and active layer thickness control. Consequently, the thickness variation of the layers over the curved surface after plasma-enhanced chemical vapor deposition (±11%) and reactive-ion etching (±12%) [17] can cause capacitance discrepancies that affects the amount of the accumulated charges on $C_{PIXEL}$ and drain voltage ($V_{DS}$) during integration ($V_{DS} = Q_{PIXEL}/C_{PIXEL}$). $V_{DS}$ should be less than $V_{GS\text{-}H} - V_{th}$, where $V_{GS\text{-}H}$ is gate voltage during readout. Thus SCAN could operate in a linear regime for both a quick readout by reducing $R_{ON}$ and a linear behavior of drain-to-source current depending on $V_{DS}$. Without changing the operation regime of SCAN, larger $C_{PIXEL}$ could increase $Q_{PIXEL}$, non-saturated $I_{TEST}$ value, and the high end of DR. Because $C_{PIXEL}$ increases along with the charge transfer time, a compromise between the charge transfer time and the dynamic range must be realized. The pixel pitch and aperture ratio also need to be taken into consideration, which is a controlling factor in the size optimization of $C_{PIXEL}$.

## 4. Conclusion

In summary, we demonstrated that LWL with a high level-to-level alignment accuracy can be used to fabricate a-Si:H TFT PPS on a hemispherical surface. We also reported electrical performance of the fabricated PPS circuits. The obtained experimental results clearly show that we can realize a high resolution a-Si:H TFT active-matrix PPS; a pixel pitch of 150 μm and a dynamic range of about 40 dB were realized in this work. By reaching a compromise between the pixel pitch and dynamic range, we can further reduce the pixel pitch to 100, 75 or 50 μm with a write head of shorter focal length in the LWL systems. Further integration of the proven solution-processable organic photodetectors will allow realizing a high resolution image sensor.

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## Biographies

**Geonwook Yoo** received his B.S. in EE from Korea University (2005), M.Eng in BME from Cornell University (2006), and is Ph.D candidate in EECS, U of Michigan. His research interests include design, simulation and layout of passive and active pixel sensor circuits with thin-film transistor (TFT) for imager. He also focuses on developing novel thin-film processes to fabricate TFT and its circuitry on curved surface.

**Tze-ching Fung** received his B.S. in physics from National Taiwan University in 2001, M.S. in EE from University of Michigan in 2005, and is a doctoral candidate in EECS, U of Michigan. His research project focuses on science and technology related to oxide semiconductor thin-film transistors (OS-TFTs). The long term goal for the project is to develop proper architecture for OS-TFTs to be used in high performance flat-panel display or photo imager.

**Daniela Radtke** received her diploma in physics in 2005 from the Friedrich-Schiller-University in Jena. Since then, she has been working at the microoptical systems department of the Fraunhofer Institute for Applied Optics and Precision Engineering towards her PhD, focusing on laser lithography on non-planar surfaces.

**Uwe D. Zeitner** received his diploma, PhD, and habilitation in physics in 1995, 1999, and 2008, respectively, from the Friedrich-Schiller-University Jena. He worked at this university in the field of fabrication of micro-optical elements and systems by e-beam lithography. Since 1999 he is with the Fraunhofer Institute of Applied Optics and Precision Engineering (IOF), Jena. His field of work is optical design and micro-lithographic fabrication techniques. He is particularly interested in the application of micro-optical elements in various fields like laser-resonators and laser systems, miniaturized optical sensor systems, and ultra-short laser-pulse shaping. Since 2006 he is heading the Center for Advanced Micro- and Nano-Optics at the IOF.

**Jerzy Kanicki** received his Ph. D. degree in sciences (D. Sc.) from the Free University of Brussels (Universite Libre de Bruxelles), Brussels, Belgium, in 1982. He subsequently joined the IBM Thomas J. Watson Research Center, Yorktown Heights, New York, as a Research Staff Member working on hydrogenated amorphous silicon devices for the photovoltaic and flat panel display applications. In 1994 he moved from IBM Research Division to the University of Michigan as a Professor in the Department of Electrical Engineering and Computer Science. At the present, his research interests within the Electrical and Computer Engineering (ECE) division of EECS, include organic electronics, thin-film transistors and circuits, and flat panel displays technology including organic light-emitting devices.